שבלת, ישראלי, רוברטס, זיסמן ושות'
SHIBOLETH
SHIBOLETH YISRAELI ROBERTS ZISMAN & Co.
ADVOCATES & NOTARIES עורכי דין ונוטריונים

APPENDIX – MARKED UP VERSION OF PROPOSED CLAIMS

1. A computer system for transferring ~~data~~ messages between a receiving central processing unit (CPU) and a transmitting CPU by using only write operations *for the purpose of enabling a read operation only from local memory of a CPU*, *said system* comprising:
   - i) at least one receiving central processing unit (CPU) *further comprising at least a read head register, a first queue length register, and a first total read register;*
   - ii) at least one transmitting CPU *further comprising at least a write head register, a second total read register, a total write, and a second queue length register;*
   - iii) a local memory for receiving CPU;
   - iv) a local memory for transmitting CPU;
   - v) means for connecting between receiving CPU and ~~second~~ *transmitting* CPU where such means transfers write operations faster than read operations; ~~and~~
   - vi) a circular queue defined between designated addresses in said local memory of said receiving CPU; *and*
   - vii) *means for adding and updating at least a separator between messages, wherein a read operation of said receiving CPU is achieved when said transmitting CPU performs:*
     - *a) a write operation of a separator to a local memory of said receiving CPU, pointed to by said write header; and*
     - *b) a write operation of at least one message to the local memory of said receiving CPU pointed to by said write header,*

       such that said receiving CPU reads said at least one message from its own local memory from a location pointed to by said read head register, and said second total read register is thereafter updated.

~~2. A computer system for transferring data between a receiving central processing unit (CPU) and a transmitting CPU by using only write operations, according to claim 1, further comprising at least one receiving control register for control of said queue, allocated in said local memory of said receiving CPU.~~

~~3. A computer system for transferring data between a receiving central processing unit (CPU) and a transmitting CPU by using only write operations, according to claim 1, further comprising at least one register for control of said queue, said at least one register being allocated in said local memory of said transmitting CPU.~~

4. The system of claim 1 wherein said means for connecting between said CPUs is a PCI bus.

~~5. The system of claim 2 where said at least one control register in said receiving memory is a receiving total read register, which contains a first copy of the total quantity of data read from said queue by said receiving CPU.~~

~~6. The system of claim 5 where said at least one control register in said receiving memory further comprises a total write register, which contains the total quantity of the data written into said queue of said receiving CPU by said transmitting CPU.~~

e-mail: manager@shibolet.com

שבלת, ישראלי, רוברטס, זיסמן ושות'
SHIBOLETH
SHIBOLETH YISRAELI ROBERTS ZISMAN & Co.
ADVOCATES & NOTARIES עורכי דין ונוטריונים

~~7. The system of claim 3, where said at least one control register in said transmitting memory further comprises a write head register, which contains a pointer to the location of the next write into said queue.~~

8. The system of claim ~~7~~1 where said ~~at least one control register in said receiving memory further comprises a transmitting~~ first total read register ~~is used to update said second total read register which contains a second~~ with a copy of the total quantity of data read from said queue by the receiving CPU.

~~9. The system of claim 5 where said at least one control register in said receiving memory further comprises a read head register, which contains a pointer to the location of the next read from said queue.~~

10. The system of claim ~~9~~1 where said ~~pointer for the next~~ read ~~head register from said queue~~ and said ~~pointer for the next~~ write ~~head register into said queue~~ are set to point to the same address upon initialization.

11. The system of claim 1~~0~~ where a maximum length is ~~specified for said~~ imposed on a message to be written into said queue.

12. The system of claim 11 where a tail is added at the end of said queue ~~said tail being~~ equal ~~in length~~ to said maximum length ~~for said~~ imposed on a message.

13. The system of claim 1~~2~~ where a message separator is used to indicate the end of said message.

14. The system of claim 13 where said message separator contains the length of ~~said~~ the immediately following message.

15. The system of claim 13 where said message separator contains a predefined "magic" number.

16. The system of claim 15 where, if said message separator contains an erroneous "magic" number, an error message is generated.

17. The system of claim 13 where said message separator of the last message in said queue is a stopper designator, and is different from said message separator between messages.

18. The system of claim 17 where said stopper designator further contains a predefined "magic" number.

19. The system of claim 18 where, if a stopper designator contains an erroneous "magic" number, an error message is generated.

e-mail: manager@shiboleth.com